WHAT IS CLAIMED IS:

1. A non-volatile semiconductor storage device comprising:

a NAND column having a plurality of memory cell transistors connected in series by a current passage;

a plurality of word lines connected to gates of the plurality of memory cell transistors in the NAND column;

word line drive circuits which drive the plurality of word lines;

a bit line connected to one end of the NAND column via a selection gate transistor;

a bit line drive circuit which drives the bit line;

a source line connected to the other end of the NAND column via a selection gate transistor;

a source line drive circuit which drives the source line; and

a potential supply circuit which supplies a potential to a semiconductor region in the NAND column in which the plurality of memory cell transistors are formed;

wherein in deletion verification which verifies that the contents stored in the plurality of memory cell transistors have been deleted, a read is executed on each of the plurality of word lines, and in the read, the word line drive circuit provides the selected

one of the plurality of word lines with a determination potential used to determine whether or not the contents have been deleted, while providing the other non-selected word lines with a read potential higher than the determination potential.

2. A non-volatile semiconductor storage device according to claim 1, wherein in the deletion verification, the potential supply circuit sets the potential in the semiconductor region in which the plurality of memory cell transistors are formed, to be higher than the determination potential.

3. A non-volatile semiconductor storage device according to claim 1, wherein after the contents stored in the memory cell transistors have been deleted, the threshold voltages of the memory cell transistors are lower than the determination voltage.

4. A non-volatile semiconductor storage device according to claim 1, wherein in the read during the deletion verification, whether or not the contents stored in the memory cell transistors have been deleted is determined depending on whether or not charges accumulated in the bit line have been discharged.

5. A non-volatile semiconductor storage device according to claim 4, wherein time required for the charges accumulated in the bit line to be discharged is shorter than time required for the charges accumulated in the bit line to be discharged during a normal read.

6. A non-volatile semiconductor storage device according to claim 1, wherein in the read during the deletion verification, the read potential provided to the non-selected word lines is lower than a potential provided to the non-selected word lines during a normal read.

7. A non-volatile semiconductor storage device according to claim 1, wherein the memory cell transistor includes a stacked structure in which a floating gate, a second gate insulating film, and a control gate are stacked on a silicon substrate via a first gate insulating film in this order.

8. A non-volatile semiconductor storage device comprising:

a NAND column having a plurality of memory cell transistors connected in series by a current passage;

a plurality of word lines connected to gates of the plurality of memory cell transistors in the NAND column;

word line drive circuits which drive the plurality of word lines;

a bit line connected to one end of the NAND column via a selection gate transistor;

a bit line drive circuit which drives the bit line;

a source line connected to the other end of the NAND column via a selection gate transistor;

a source line drive circuit which drives the source line; and

a potential supply circuit which supplies a potential to a semiconductor region in the NAND column in which the plurality of memory cell transistors are formed;

wherein the word line drive circuits supply a low voltage to the plurality of word lines, wherein the potential supply circuit supplies a high potential higher than the low potential, to the semiconductor region in which the plurality of memory cell transistors are formed, to delete contents stored in the plurality of memory cell transistors, and

wherein in deletion verification which verifies that the contents stored in the plurality of memory cell transistors have been deleted, a read is executed on every predetermined number of word lines of the plurality of word lines, the number of the predetermined number of word lines being at least two and smaller than the total number of word lines, and in the read, the word line drive circuit provides the selected ones of the plurality of word lines with a determination potential used to determine whether or not the contents have been deleted, while providing the other non-selected word lines with a read potential higher than the determination potential.

9. A non-volatile semiconductor storage device

according to claim 8, wherein in the deletion verification, the potential supply circuit sets the potential in the semiconductor region in which the plurality of memory cell transistors are formed, to be higher than the determination potential.

10. A non-volatile semiconductor storage device according to claim 8, wherein after the contents stored in the memory cell transistors have been deleted, the threshold voltages of the memory cell transistors are lower than the determination voltage.

11. A non-volatile semiconductor storage device according to claim 8, wherein in the read during the deletion verification, whether or not the contents stored in the memory cell transistors have been deleted is determined depending on whether or not charges accumulated in the bit line have been discharged.

12. A non-volatile semiconductor storage device according to claim 11, wherein time required for the charges accumulated in the bit line to be discharged is shorter than time required for the charges accumulated in the bit line to be discharged during a normal read.

13. A non-volatile semiconductor storage device according to claim 8, wherein in the read during the deletion verification, the read potential provided to the non-selected word lines is lower than a potential provided to the non-selected word lines during a normal read.

14. A non-volatile semiconductor storage device according to claim 8, wherein the memory cell transistor includes a stacked structure in which a floating gate, a second gate insulating film, and a control gate are stacked on a silicon substrate via a first gate insulating film in this order.

15. A deletion verification method for a non-volatile semiconductor storage device having a NAND column having a plurality of memory cell transistors connected in series by a current passage and a plurality of word lines connected to gates of the plurality of memory cell transistors in the NAND column, the method comprising:

supplying a low potential to the plurality of word lines, while supplying a high potential higher than the low potential, to a semiconductor region in which the plurality of memory cell transistors are formed, to delete contents stored in the plurality of memory cell transistors; and

executing a read on each of the plurality of word lines, and in the read, providing the selected one of the plurality of word lines with a determination potential used to determine whether or not the contents have been deleted, while providing the other non-selected word lines with a read potential higher than the determination potential.

16. A deletion verification method for a

non-volatile semiconductor storage device according to claim 15, wherein in the deletion verification, the potential in the semiconductor region in which the plurality of memory cell transistors are formed is set to be higher than the determination potential.

17. A deletion verification method for a non-volatile semiconductor storage device according to claim 15, wherein after the contents stored in the memory cell transistors have been deleted, the threshold voltages of the memory cell transistors are lower than the determination voltage.

18. A deletion verification method for a non-volatile semiconductor storage device according to claim 15, wherein in the deletion verification, whether or not the contents stored in the memory cell transistors have been deleted is determined depending on whether or not charges accumulated in the bit line have been discharged.

19. A deletion verification method for a non-volatile semiconductor storage device according to claim 18, wherein time required for the charges accumulated in the bit line to be discharged is shorter than time required for the charges accumulated in the bit line to be discharged during a normal read.

20. A deletion verification method for a non-volatile semiconductor storage device according to claim 15, wherein in the read during the deletion

verification, the read potential provided to the non-selected word lines is lower than a potential provided to the non-selected word lines during a normal read.

21. A deletion verification method for a non-volatile semiconductor storage device according to claim 15, wherein the memory cell transistor includes a stacked structure in which a floating gate, a second gate insulating film, and a control gate are stacked on a silicon substrate via a first gate insulating film in this order.

22. A deletion verification method for a non-volatile semiconductor storage device having a NAND column having a plurality of memory cell transistors connected in series by a current passage and a plurality of word lines connected to gates of the plurality of memory cell transistors in the NAND column, the method comprising:

supplying a low potential to the plurality of word lines, while supplying a high potential higher than the low potential, to a semiconductor region in which the plurality of memory cell transistors are formed, to delete contents stored in the plurality of memory cell transistors; and

executing a read on every predetermined number of word lines of the plurality of word lines, the number of the predetermined number of word lines being at least two and smaller than the total number of word

lines, and in the read, providing the selected ones of the plurality of word lines with a determination potential used to determine whether or not the contents have been deleted, while providing the other non-selected word lines with a read potential higher than the determination potential.

23. A deletion verification method for a non-volatile semiconductor storage device according to claim 22, wherein in the deletion verification, the potential in the semiconductor region in which the plurality of memory cell transistors are formed is set to be higher than the determination potential.

24. A deletion verification method for a non-volatile semiconductor storage device according to claim 22, wherein after the contents stored in the memory cell transistors have been deleted, the threshold voltages of the memory cell transistors are lower than the determination voltage.

25. A deletion verification method for a non-volatile semiconductor storage device according to claim 22, wherein in the deletion verification, whether or not the contents stored in the memory cell transistors have been deleted is determined depending on whether or not charges accumulated in the bit line have been discharged.

26. A deletion verification method for a non-volatile semiconductor storage device according to

claim 25, wherein time required for the charges accumulated in the bit line to be discharged is shorter than time required for the charges accumulated in the bit line to be discharged during a normal read.

27. A deletion verification method for a non-volatile semiconductor storage device according to claim 22, wherein in the read during the deletion verification, the read potential provided to the non-selected word lines is lower than a potential provided to the non-selected word lines during a normal read.

28. A deletion verification method for a non-volatile semiconductor storage device according to claim 22, wherein the memory cell transistor includes a stacked structure in which a floating gate, a second gate insulating film, and a control gate are stacked on a silicon substrate via a first gate insulating film in this order.